**6SENG006W Concurrent Programming**

**FSP Process Analysis & Design Form**

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| **Name** |  |
| **Student ID** |  |
| **Date** |  |

**1. FSP Process Attributes**

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| **Attribute** | **Value** |
| **Name** |  |
| **Description** |  |
| **Alphabet** |  |
| **Number of States** |  |
| **Deadlocks (yes/no)** |  |
| **Deadlock Trace(s)**  **(if applicable)** |  |

**2. FSP Process Code**

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| **FSP Process:** |
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**3. Actions Description**

A description of what each of the FSP process' actions represents, i.e. is modelling. In addition, indicate if the action is intended to be synchronised (shared) with another process or asynchronous (not shared). (Add rows as necessary.)

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| **Actions** | **Represents** | **Synchronous or Asynchronous** |
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**4. FSM/LTS Diagrams of FSP Process**

Note that if there are too many states, more than 64, then the LTSA tool will not be able to draw the diagram. In this case draw small diagrams of the most important parts of the complete diagram.

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**5. LTS States**

A description of what each of the FSP process' states represents, i.e. is modelling. If there are a large number of states then you can group similar states together &/or only include the most important ones. For example, identify any states related to mutual exclusion (ME) & the associated critical section (CS), e.g. waiting to enter the CS state, in the CS state(s), left the CS state. (Add rows as necessary.)

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| **State** | **Represents** |
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**6. Trace Tree for FSP Process**

The trace tree for the process. Use the conventions given in the lecture notes and add explanatory notes if necessary.

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